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A Programmable System on Chip (PSOC) for Active Power Filter (APF) Based on Cortex M3

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***Abstract*—** The proper power distribution is more important in present days as the power demand is increasing rapidly. The parameters like reactive power and the harmonic current poses some serious problems like transformer heating, machine vibration and line losses. There is various control techniques has been adopted in recent past to overcome the above issues. The Synchronous Reference Frame (SRF) based control algorithm gives the high response as it divides both the reactive power and harmonic components. The drawback of SRF based control algorithm is that it needs proper synchronization of input current with utility voltage. The synchronization can be achieved by using the microcontroller or digital signal processing (DSP) but face fundamental challenges like high computational time, less accuracy, limited sampling time etc. This paper gives a novel PSoC by using the FPGA board, Cortex M3 board, and analog-to-digital converter (ADC), digital to analog converter (DAC) boards. In this, the existing Cypress 1/3/5 PSoC board is discussed. In order to perform the simulation over the proposed PSoC we have used the modelsim-6f and Xilinx 14.7 platforms. Also, the cathode-ray oscilloscope *(*CRO*) is used to observe the output signals.*

Keywords— *Directed Current Controller , FPGA, Harmonics, , PSoC, PWM, PLL, reactive power, SRF.*

I. INTRODUCTION

Power system plays an important role in day today's life. Thus maintaining the quality of power is much essential as per application prospective. During the power distribution harmonics may occurs due to the presence of nonlinear loads at the load side. These harmonics cause the harmonic currents in the power system because of this transformer overheating, degradation of voltage quality, machine vibration, malfunctioning of power equipments etc. To solve these harmonic issues several harmonic mitigation standards are presented, for example: IEC1000-3-4, IEEE-19, IEEE1000-3-2 etc. The harmonic current suppression done by passive/active power filters (PPF/APF). The PPF is used to minimize the line-current losses and increase the power quality. But, the PPF have drawbacks like sensitivity towards system impedance variation, sensitivity towards the source frequency variation, issues related to the resonance, the fixed filter frequency is not easily adjustable. Among these drawbacks resonance is critical issue. Thus many researchers have suggested for active power filter (APF).

The significance of the APF is that it can suppress harmonic components of different order at same time. The harmonics in a power system have various consequences like huge voltage distortion, reduction in ac motor efficiency etc. The significant feature of the APF compared to the PPF is that it is smaller in size by which helps to reduce the reactive power and harmonic current The APF act as source of harmonics current, which intended to produce the desired output by eliminating the harmonic current and obtain the reactive power [1-5].

In order to suppress the harmonics there were various techniques have been used. The technique called Digital Signal Processing (DSP) or different software based techniques have shown interest due to its computational flexibility. Apart from the computational flexibility these techniques consume huge Central Processing Unit (CPU) time, which gives computational latency. Thus, the recently developed fast processing APFs are implemented on the basis of the multi-DSP technique. Sometimes, the complete algorithm can be used over a single DSP having Low sampling rated and low time delay compensation of Low power filter (LPF). All the techniques used can bring the hardware and software design pattern complication. In some cases these techniques may deteriorate compensation accuracy and performance.

This paper presents a PSoC, consisting of analog-to-digital converter, cortex M3, FPGA board, CRO etc. The Psoc is designed by using two units like three phase-Phase Locked Loop (3φ PLL), Directed current control (DCC). Later the performance is compared by using modelsim-6f and Xilinx 14.7. The sectional partition of the paper is divided as: Section II addresses the background of APF. Section III describes the existing system. Section IV describes the problem statement. Section V illustrates the proposed PSoC system. Section VI gives the algorithm implementation. Section VII discusses the results analysis and finally Section III gives the conclusion.

II. BACKGROUND

The APFs implemented for suppression of the different ordered harmonic components caused by nonlinear loads. Based on the connections and circuit configurations, APF classified as series, parallel and hybrid.

Parallel APF: This is connected to the load in parallel which gives the compensation current that stops the load harmonic current feeding into the feeder. This filters composed with various configurations [6], in this we have described the standard inverter type APF (SIAPF).

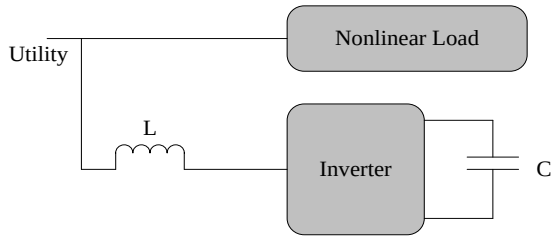

Figure1: System Configuration of Conventional Parallel APF

The figure 1 represents the standard inverter (SI) type parallel APF [7, 8]. This APF can suppress harmonic current 3φ current balancing and compensation of reactive power. This APF consists of a voltage-source (V-S) power converter and filter inductor connected in series. The functionality of filter inductor (FI) is to suppress higher frequency ripple current occurred due to power converter switching. The inductance of FI depends on dc voltage, ripple current and switching frequency. The dc bus voltage should be greater than the peak utility voltage to actuate APF output current at compensating current command in parallel APF. The greater dc bus voltage utilization has also got various drawbacks like greater filter inductance and dc capacitor voltage rating [9]. A greater FI results significant power loss, larger heat dissipation, enhances the size and weight and decreases the frequency response performance. The need of greater dc capacitor voltage rating and other electronic devices limits high power application of APFs because of cost and greater power rating [10, 11].

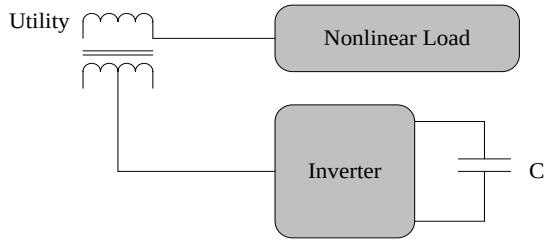

Figure 2: System Configuration of Conventional Series APF

The figure 2 shows series APF system configuration. The series APF advantage over the parallel APF is that it can maintains the output. The figures 1 (a) shows SI parallel APF configuration, (b) series APF configuration, (c) hybrid APF configuration. The voltage waveform must be sinusoidal and balance the 3φ voltages. But, the series APF is not used in industrial applications because of its series circuits, i.e, it should handle high load currents, that enhances their current rating in comparison with the parallel APF [12].

The combinations of different of filters can offer better significances. Among these combinations, parallel APF and series APF and parallel passive APF, parallel APF and parallel passive filter, and APF in series with parallel passive APF are widely used [13]. The combination of APF in series with parallel, called as hybrid APF.

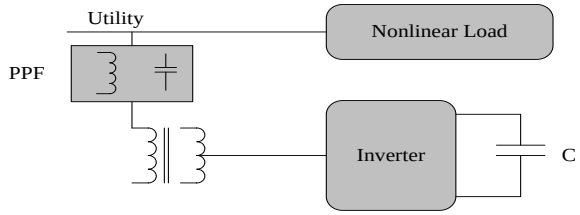

Figure3: System configuration of hybrid APF

The figure 3 shows the passive APF configuration, which filters the dominant harmonic, and the power converter implemented for enhancement of the filter performance and for passive filter protection against the power resonance. Thus, power converter capacity is less than the parallel APF at nonlinear load condition. Also, the voltage stress applied for power electronic switches within power converter is low. Hence, hybrid filter are used in high-power applications. But hybrid APF needs a huge passive APF set and also, a voltage-matching transformer. The APF can be divided into reactive power compensation, 3φ systems balancing, multiple compensations, and harmonic compensation. The basic parallel APF is multiple compensations type which compensate for the reactive power and harmonic current simultaneously. The hybrid APF is of harmonic compensation type, which compensates only for the harmonic current [10]–[14].

III. EXISTING SYSTEM

Currently, there is PSoC from Cypress which has several significant configurations and are discussed below. This PSoC is a product of Cypress, which gives an idea developing capable products for variety of applications. The PSoC is a programmable chip, which integrates configurable digital peripheral and analog functionalities, memory and microcontroller in a single chip [15].

Figure 4: PSoC development board (Cy8cKit)

Figure 5: PSoC family processor module (Cy8c29)

The above figure 4, gives the existing PSoC development kit from Cypress 135 of model "Cy8cKit-001" which provides a single platform for development of various prototype and evaluation of various solutions by using all the PSoC architectures from PSoC 1 to 5. This board offers a better flexibility for power domain configurations. The board consists of three linear regulators and are can be utilized for PSoC modules and power peripherals with voltage range from 1.7V to 5.0V. The boards also got the ability of separating the PSoC drain supply rail into analog and digital rails. Also, it has got capability of separating the input/output drain voltage rails by giving flexibility for input/output ports at variable voltage condition. The board contains a LCD module that gives the alphanumeric display output. The board is included with an USB interface and wireless interface module. The board consists of an breadboard which has complete input/output sockets, push button, LED's and variable resistor. Also the board is designed with modularity by which various processing modules can be installed and a desired module can be selected by the board depending on the PSoC1,3 and 5 device features. A PSoC development board consists of various modules and blocks in below figure 3, a PSoC family processor module is shown. In, figure 3, the processor module consists of family processor module, and it can be utilized in interface with the PSoC (Cy8ckit-001) for development of designs using over the on board development kit resources or compatibility expansion boards. The family kit gives the extra processor modules to use over the various projects.

The following figure shows the complete PSoC development kit (version: 1/3/5) that supports all PSoC architectures.


Figure 6: Complete PSoC development kit

IV. PROBLEM STATEMENT

In the power distribution system the RP and the harmonic current may offer some of the serious issues causing transformer heating, line losses, malfunctioning of power equipments and machine vibration [16,17, 18].

- In recent years, some of the control mechanisms are presented and studied. Among various researches, Synchronous Reference Frame (SRF) based control algorithm is highly considered theory as it is simpler and offer good response.
- The SRF based control algorithm (SRFCA) will give capability to decompose or separate the components of RP and harmonics of distortion currents.
- The SRFCA needs utility voltage phase information and hence a synchronizer is must to describe the proper synchronization of source currents with the utility voltages. Thus, different auxiliary algorithms like protection module, dc voltage regulator, ADC drivers and directed-current (d-c) controller etc., are required to be implemented.
- Thus, these overall complicated steps are cause problem in digital controller realization, mainly in a system with high sampling rate.
- A approach with digital signal processing (DSP) or other software oriented methods can offer better flexibility and computational ability. But, the each subsystems subjected to the control algorithm holds CPU time and which causes computation latency.
- Hence, the fast processing APFs are used on the basis of multi-DSP mechanism or of single-DSP with whole algorithm implementation by using low pass filter (LPF) of low sampling rate and time delay compensation.

Thus, all the above solutions can offer complication while designing hardware and software and also may cause the reduction of compensation accuracy and dynamic performance. Thus, the implementation of PSoC based control algorithms will execute all the above stated procedures/steps simultaneously with hardware implementation.

V. PROPOSED SYSTEM

The proposed PSoC system consists of hardware components like Cortex-M3 that consists of ADC, FPGA consists of PLL unit and DAC and CRO for output display.

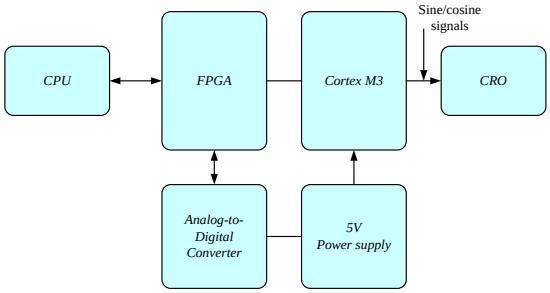

Figure 7: Architecture of proposed PSoC system

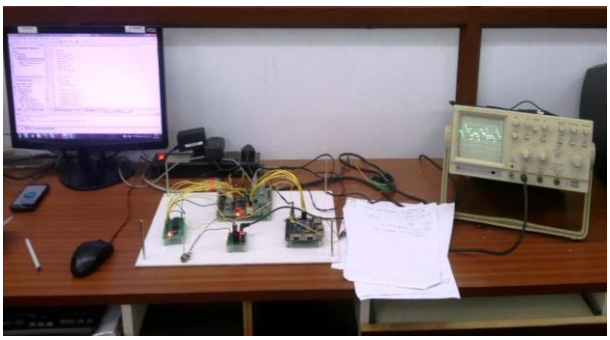

Figure 8: Experiment set up PSoC system

In figure.8, architecture of proposed PSoC system is presented. The figure 6, gives the experimental setup. In this, Xilinx.14.7 and modelsim-6f is used for simulation. The CPU unit of computer is connected with FPGA board by using Jtag cable. Also, PSoC system is supplied with 5V supply.

VI. CIRCUIT IMPLEMENTATION

The FPGA unit in the proposed PSoC system consists of 3-phase PLL system and a Directed current controller unit. These units are implemented as below.

A. 3-phase PLL system

The PLL system consists of input voltage (Vd_trans), PI controller, 8bit adder generator, and sine table and post processor. The PLL system operation gives the cosine and sine signal outputs. The algorithm for PLL system is given below.

Algorithm for PLL system:
Input: 3-phase input voltages (Va,Vb and Vc)
Output: cosine, sine signal.
Start
Step-1: Consider Va, Vb, Vc
Step 2: Assume Vdr=0 at PLL condition, attain Vd=Δ
Step-3: Transfer Vd to PI controller
Step-4: Multiply Δ with Kp and Ki
Step-5: Add Np and Ni shifters to PI controller "add"
Step-6: Use Sine Table and post process
Step-7: Obtain "sine/cosine" output
End

The PLL system provides cosine/sine output signals from the input voltages (Va, Vb and Vc). After considering the inputs (step-1), the reference voltage Vdr is assumed as zero in normal operating condition and achieved a voltage Vd= Δ, where Δ represents the loop error (step-2). This Vd is transferred to PI controller (step-3). Later, the constants like Kp and Ki are multiplied with Δ to perform the shifting operation (step-4). The shifter Np and Ni are added to PI controller and the output of it is given to 8bit Adder generator (stp-5). At next, the generated signals will be subjected to Sine table and post processing (step-6) is performed to get the sine/cosine outputs (step-7).

Algorithm for directed current controller
Input: R_i
Output: PWM
Start
Step-1: Define 3φ R_i
Step-2: Convert "3φ R_i*" to "*2φ R_i"
Step-3: Generate "Magm" from 2φ R_i
Step-4: Generate "Si" by decoder table
Step-5: Combine "Magm+Si"
Step-6: Get PWM
End

The algorithm for hardware implementation, gives the detailed block of hardware implementation. In first step we consider 3φreference input i.e. Ri . In step 2 the Ri , is converted to 2φ by using the shifter (Sh) and adders (ad) shown in figure 7. Later, magnitude module (Magm) and sector identification (Si) is generated using 2φ and decoder respectively. Then the generated outputs are applied to generate pulse width modulation (PWM) outputs by using the switching generators (Sg) and switching table (St).

VII. RESULTS ANALYSIS

The outcome of the proposed study is simulated using soft-computational approach using modelsim 6.3f and Xilinx 14.7 and Spartan 3 FPGA, cortex M3, ADC combined PSoC board.

A. Experimental set up outcomes:

This section gives the various parts of working PSoC system. The collaborative model of PSoC system is given in figure7, which contains analog-digital Converter (ADC) board, supply unit, FPGA, Cortex M3 board. The 5V supply is given to ADC and cortex M3 while the FPGA is supplied with direct power supply. Also a load unit is given through which signals are adjusted. In the below figure 7, the ADC is interfaced with FPGA and load. The FPGA is connected to CPU & Cortex M3 board.

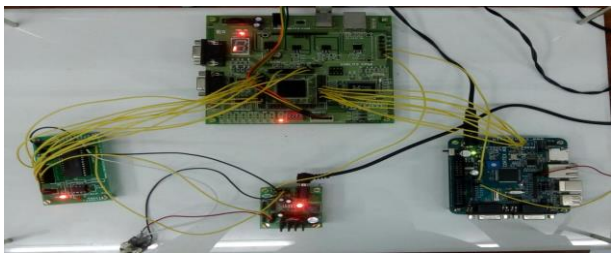

Figure 9: working PSoC system

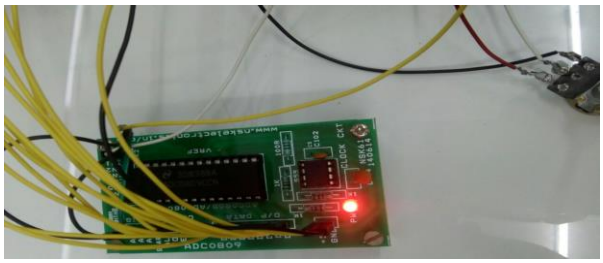

Figure 10: ADC board operation

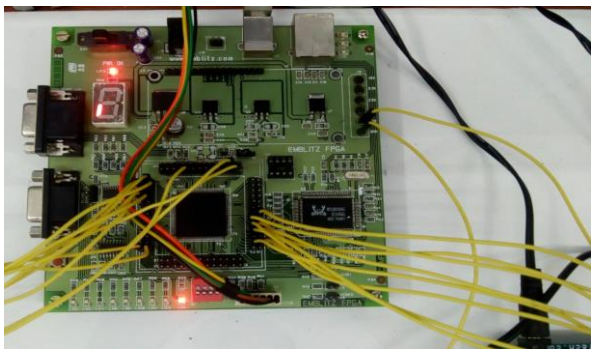

Figure 11: FPGA board operation

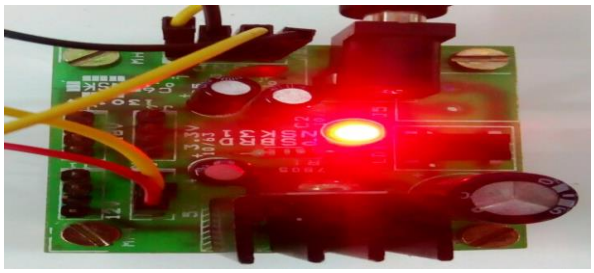

Figure 12: Supply unit operation

Figure 13: Cortex M3 board operation

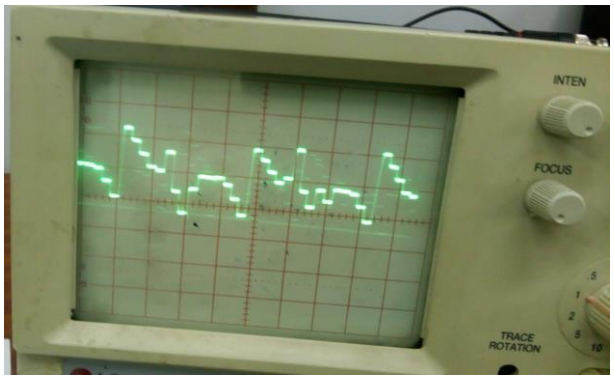

Figure 14: Output signals

B. Reseults discussion

In this section, we have discussed the various outcomes achieved by varying the load, modelsim-6f and Xilinx 14.7.

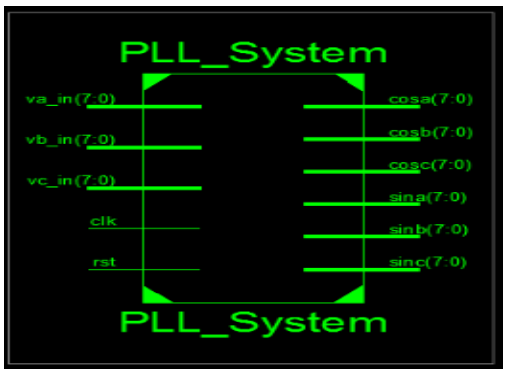

Figure15: RTL Schematic of PLL system

The above figure 15, shows the RTL schematic of PLL system, where inputs are va_in (7.0), vb_in (7.0), vc_in (7.0), clock and reset) and the outputs are (cosa(7.0), (cosb(7.0), (cosc(7.0), sina(7.0), sinb(7.0) and sinc (7.0)).

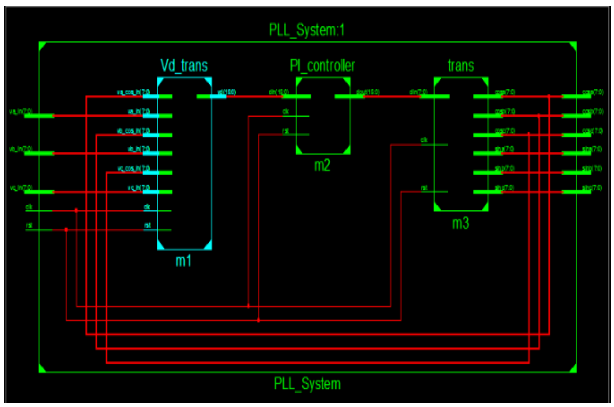

Figure 16: Top module of PLL system

The above shows the top module of PLL system that consists of Vd_transmission inputs, PI controller and output transmission.

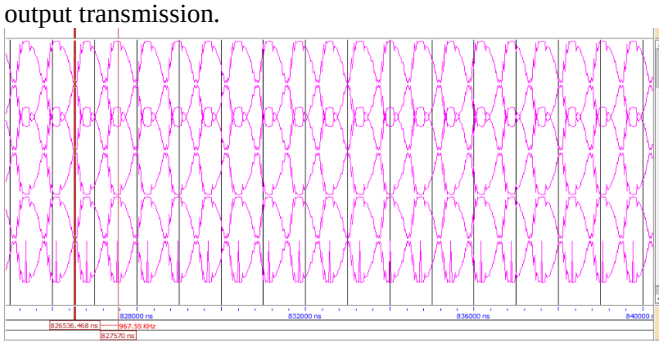

Figure 17: Simulation outcome of PLL system

The above figure 17 shows the simulation outcome of the PLL system.

PLL_System Project Status (12/28/2016 - 16:16:09)			
Project File:	test1.xise	**Parser Errors:**	No Errors
Module Name:	PLL_System	**Implementation State:**	Synthesized
Target Device:	xc3s400-5pq208	• **Errors:**	
Product Version:	ISE 14.7	• **Warnings:**	
Design Goal:	Balanced	• **Routing Results:**	
Design Strategy:	Xilinx Default (unlocked)	• **Timing Constraints:**	
Environment:	System Settings	• **Final Timing Score:**	

Device Utilization Summary (estimated values) [-]			
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slices	84	2448	3%
Number of Slice Flip Flops	59	4896	1%
Number of 4 input LUTs	120	4896	2%
Number of bonded IOBs	37	108	34%
Number of MULT18X18SIOs	2	12	16%
Number of GCLKs	1	24	4%

Figure18: Device utilization outcome

In figure 18 the utilized slices are of 3%, slice flip flops are of 1%, the number of input LUTs are utilized of 2%, IOB's of 34%, GOLKs of 4% and Multi IOs of 16%.

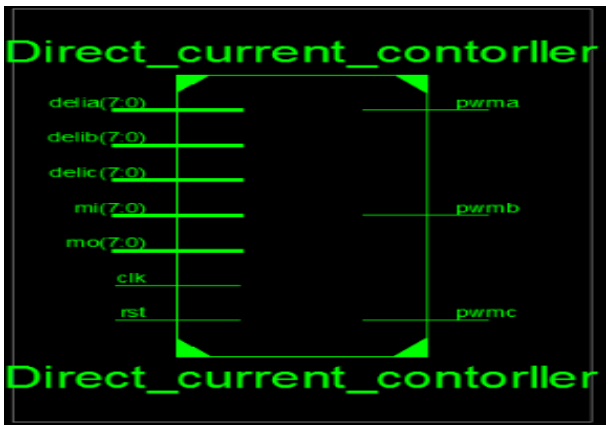

Figure 19: RTL Schematic of direct current controller

The above figure 19 shows the RTL schematic of directed current controller, where inputs are delia (7.0), delib (7.0), delic (7.0), mi (7.0), mo (7.0), clock and reset and the outputs are PWMs pwma, pwmb and pwmc.

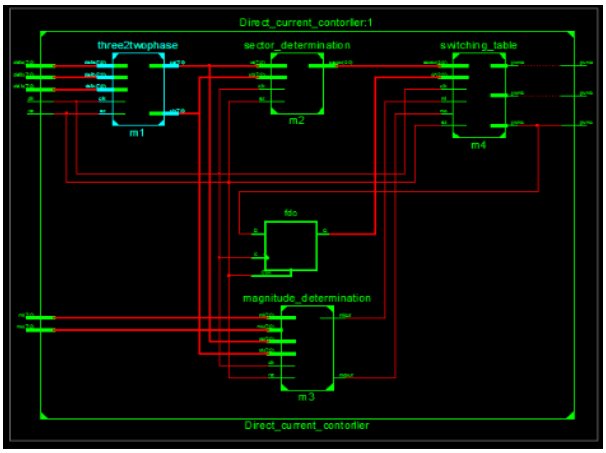

Figure 20: Top module of directed current controller

The above shows the top module of directed current controller that consists of units like sector determination, magnitude determination, switch table and 3φ to 2φ.

Figure 21: Simulation outcome of directed current controller

Direct_current_contorller Project Status (12/28/2016 - 17:11:51)			
Project File:	test1.xise	**Parser Errors:**	No Errors
Module Name:	Direct_current_contorller	**Implementation State:**	Synthesized
Target Device:	xc3s400-5pq208	• **Errors:**	
Product Version:	ISE 14.7	• **Warnings:**	
Design Goal:	Balanced	• **Routing Results:**	
Design Strategy:	Xilinx Default (unlocked)	• **Timing Constraints:**	
Environment:	System Settings	• **Final Timing Score:**	

Device Utilization Summary (estimated values) [-]			
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slices	151	3584	4%
Number of Slice Flip Flops	97	7168	1%
Number of 4 input LUTs	291	7168	4%
Number of bonded IOBs	74	141	52%
Number of MULT18X18s	1	16	6%
Number of GCLKs	1	8	12%

Figure 22: Device utilization outcome of directed current controller

In figure 22, the utilized slices are of 4%, slice flip flops are of 1%, the number of input LUTs are utilized of 4%, IOB's of 52%, GOLKs of 12% and Multi IOs of 6%.

VIII. CONCLUSION

This paper is intended to design an PSoC system that can deliver a better results like existing Cypress PSoC system. The proposed PSoC system consists of analog-digital Converter (ADC) board, supply unit, FPGA and Cortex M3 board. The 5V supply is given to ADC and cortex M3 while the FPGA is supplied with direct power supply. Also a load unit is given through which signals are adjusted. The generated signals were observed in CRO display. For simulation we have used Xilinx 14.7, modelsim-6f and the obtained results shows the optimized results in hardware implementation and response. The main advantage proposed PSoC is that it is reconfigurable and it can offer better performance for APF.

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